

FABRICATION TECHNIQUES FOR X-BAND MONOLITHIC VCOs

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ABSTRACT

Monolithic GaAs FET VCOs have been designed and fabricated utilizing a submicron-gate FET, wide-capacitance-ratio varactor diodes, MIM capacitors, microstripline inductors, resistors and air-bridge interconnections on a single GaAs chip. Design considerations and fabrication techniques for each of these components are given.

MONOLITHIC CIRCUIT ELEMENTS

As published previously^{1,2}, GaAs monolithic VCOs have been built which provide wide tuning bandwidth in X- and Ku-bands. Figure 1 is a photograph of such an MMIC chip

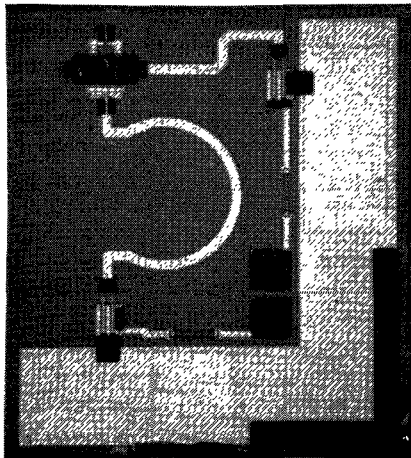


Figure 1. Monolithic VCO

illustrating the following monolithic circuit elements: a low parasitic submicron FET, two lateral, wide-capacitance-ratio varactor diodes, transmission line inductors, bypass capacitors, bias chokes and resistors.

GaAs FET

The power generating device used in this monolithic circuit is a 300 μm gate width GaAs FET with four 0.5 μm x 300 μm gate fingers. Figure 2 is an SEM photograph of this

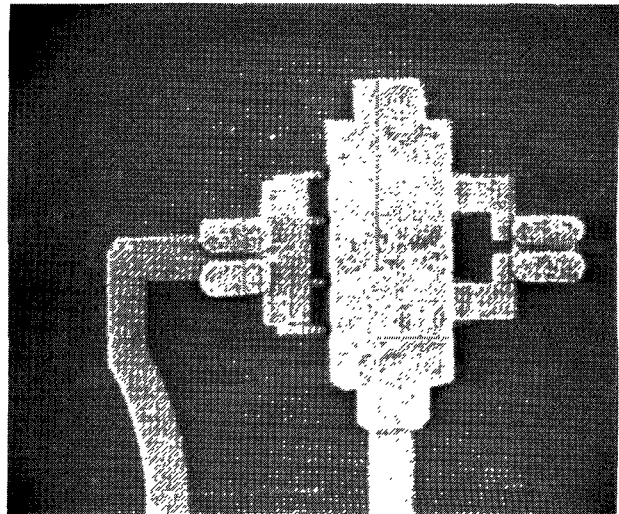


Figure 2. Low Parasitic Monolithic FET

device. The source regions are of minimum size and are interconnected with air bridges to minimize parasitic capacitance from source to ground. This capacitance is unimportant in devices used as common-source amplifiers, but for oscillators it can limit tuning bandwidth. This circuit uses e-beam lithography for the FET gate and the varactor anode. This technique allows flexibility in programming the gate and anode size. The FET is designed so that only two of the four gate fingers can be exposed to produce a 150 μm gate width device. In addition, the gate and drain pads are split; one-half of each pad is used for the 150 μm device. These

pads are interconnected by gate metal and the other two gate fingers are defined when a 300 μm device is required. The smaller gate width device along with a smaller area varactor anode (achieved by defining narrower or shorter anode fingers) are used for frequencies above 20 GHz. This higher frequency resonance is the result of the series connection of the fixed inductor and the smaller gate and varactor capacitances.

Lateral Varactor Diodes

Figure 3 shows the two-finger lateral varactor diode used in this circuit. Each

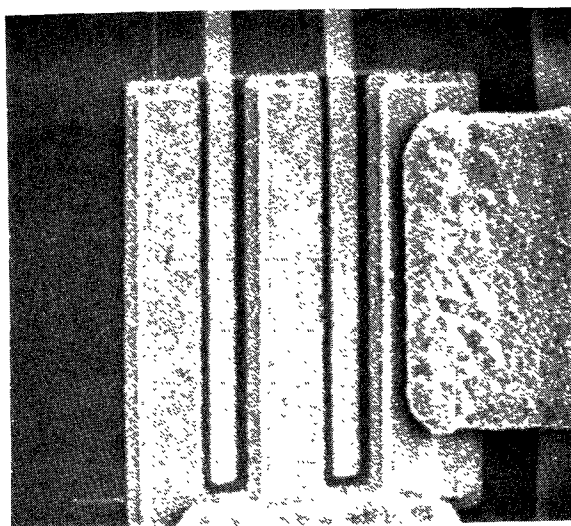


Figure 3. Monolithic Lateral Varactor Diode

finger is 6 μm x 75 μm resulting in a zero-bias capacitance of approximately 1 pF on a $1.5 \times 10^{17} \text{ cm}^{-3}$ layer. When recessed approximately 30% to obtain a 4 V punch-through voltage, the capacitance ratio for this device is predicted to be 34:1 based on a transmission line model of the lateral rf current flow under the anode³. Actual CV characteristic of these devices has closely matched theory. Figure 4 gives the theoretical CV and Q versus V characteristic for this diode. Note that a sharp drop in Q is observed just before punch-through and very high Q after punch-through. This unique loss characteristic explains why these circuits to date have ceased to oscillate at varactor bias voltages near punch-through. Future circuits will use narrower anode fingers (at the expense of capacitance ratio) to improve the Q.

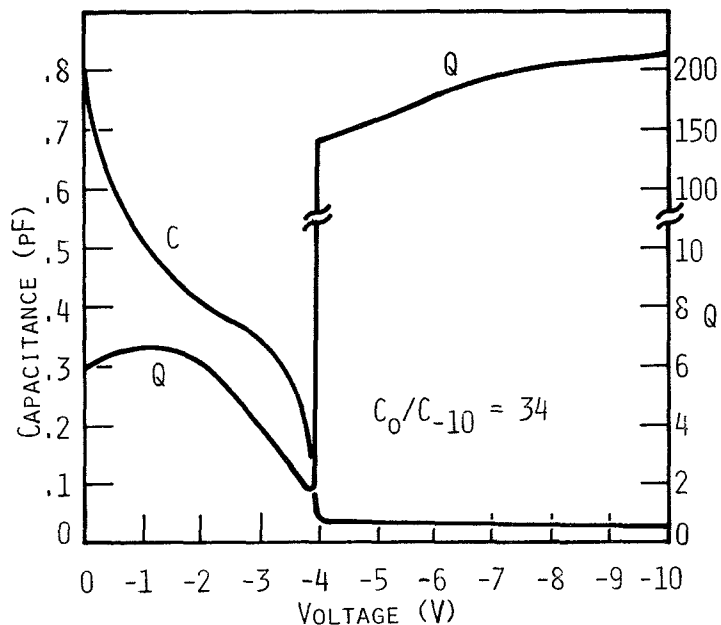


Figure 4. Theoretical CV and QV Characteristics of Lateral, Punch-Through Varactor Diode

Another factor limiting tuning bandwidth on the present circuits has been low varactor diode breakdown voltage. Since the varactor anode and the FET gate are recessed the same amount into the same active layer, they have similar breakdown voltages. The rf voltage swing on the FET gate under oscillating conditions is quite large. As a result, the rf voltage swing on the varactor is a substantial fraction of its punch-through voltage. The effective capacitance ratio before breakdown is therefore lower than expected merely from dc bias considerations. Improved performance would be obtained by using lower doping and higher punch-through voltage for the varactor than for the FET. Selective implantation can be used to provide mid- 10^{16} cm^{-3} doping under the varactor with only a minor increase in process complexity.

Transmission Lines/Inductors

The inductive reactance used in these VCO circuits is achieved using high impedance microstrip lines less than one-tenth wavelength long. The reactance of these lines is modelled using COMPACT but can be fairly accurately estimated assuming 6 nH/cm for 25 μm wide lines on 200 μm thick GaAs. The characteristic impedance of these lines is

90 Ω and loss is 0.25 dB per cm. Lines 12 μm wide (110 Ω) are used as bias lines. Figure 5 shows a section of one of these microstrip transmission lines. It was

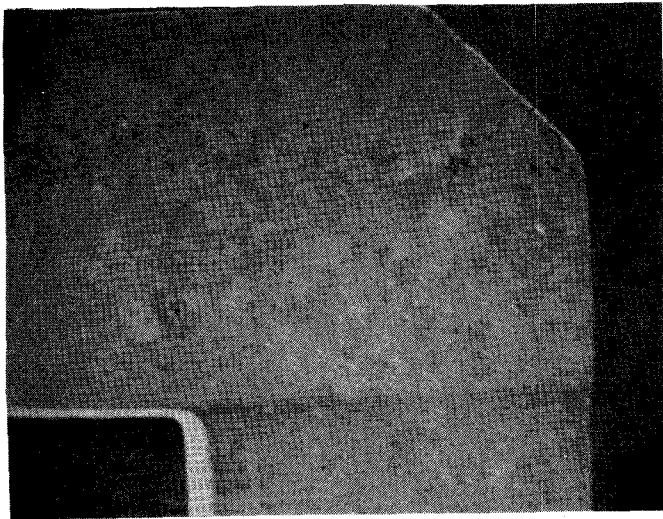


Figure 5. Microstrip Transmission Line

fabricated using dielectric-assisted lift-off of Ti/Au. The gold thickness is 1.6 μm , more than two skin depths in X- and Ku-bands. Quite good dimensional control and edge definition is obtained using this technique. The loss of these inductors is comparable to that of the same size inductors using thicker electroplated gold. This loss was determined by making Q measurements on monolithic LC test structures. Q's greater than 20 were obtained for 1.5 nH inductors resonating with 0.25 pF capacitors near 10 GHz.

Monolithic Resistors

Figure 6 shows one end of a 3K Ω monolithic GaAs resistor. It is fabricated by mesa etching the GaAs active layer and forming ohmic contacts to the ends. Knowing that the sheet resistance of the epitaxial layer is 400 ohm per square, the size of this resistor was designed to be 12 μm x 100 μm . The value of this resistor is not critical since it is merely used to suppress bias circuit oscillations, but ion implanted or anodically thinned layers provide sheet resistances within $\pm 10\%$. These sheet resistance values comprehend the fact that a surface depletion layer normally exists at the GaAs surface, and in fact, we have found this surface depletion layer to be quite stable once the silicon nitride passivation is

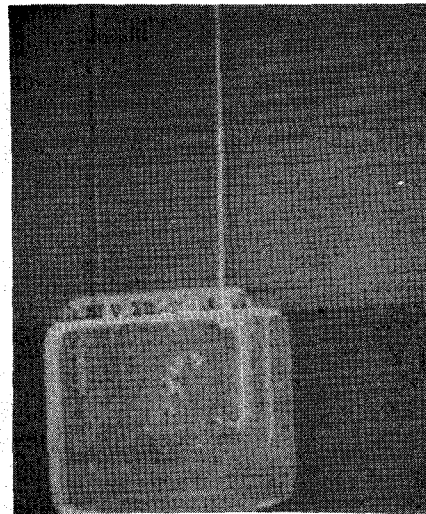


Figure 6. Monolithic GaAs Resistor

deposited. The temperature coefficient of resistance for these resistors is +1900 ppm/ $^{\circ}\text{C}$. Such a high value would be undesirable for some applications but presents no problem in this circuit.

MIM Capacitors

Capacitors used for rf bypass in this circuit are 15 pF capacitors fabricated by depositing 3000 \AA of silicon nitride over the 1.6 μm gold bottom plate which is the same gold layer which forms the transmission lines in other parts of the circuit. The top capacitor plate is another Ti/Au layer with 0.5 μm of gold. Thus low-loss metallization is used for both capacitor plates. The silicon nitride is deposited at 250 $^{\circ}\text{C}$ using a plasma-assisted CVD process. The capacitance per unit area is 0.12 pF/mil² (7.74×10^{-7} pF/cm²) with a corresponding dielectric constant of 6.3. Silicon nitride thickness repeatability is maintained to $\pm 5\%$ and yields greater than 90% for capacitors of this size are typically obtained. The temperature coefficient of capacitance for these capacitors is quite low at +75 ppm/ $^{\circ}\text{C}$.

Since both top and bottom capacitor metallizations are defined by a lift-off process, nearly vertical and occasionally ragged metal edges are obtained. To obviate problems with nitride and metal continuity across these edges, an air bridge is used to connect from the capacitor top plate to the varactor diode cathode. This electroplated bridge is shown in Figure 7. Note that

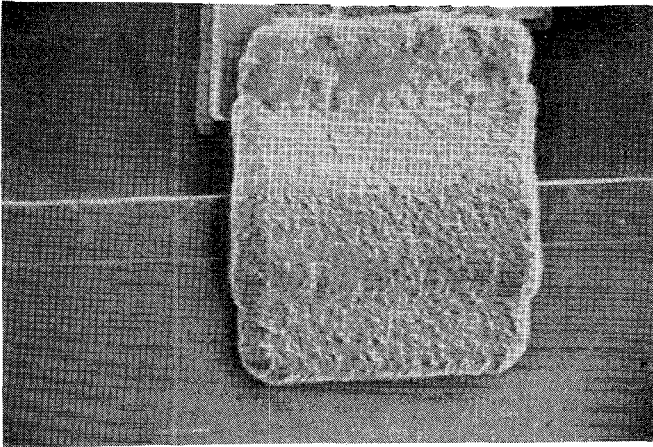


Figure 7. Monolithic Capacitor with Air Bridge Interconnect

although the capacitor metal edges are quite smooth and well-defined, they are nearly vertical in cross section.

Conclusions

The design and fabrication of high performance, low parasitic circuit elements used in the monolithic X- and Ku-band voltage controlled oscillator have been demonstrated.

Acknowledgements

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